Single-Channel Gate Driver for Enhancement Mode GaN Transistorsr

FEATURES

- Independent Source and Sink Outputs for Controllable Rise and Fall Times
- Fast Propagation Delays (11ns Typical)
- Fast Rise and Fall Times (13.4ns,8.4ns Typical)
- Integrated LDO for Adjustable Gate Driver Output Voltage Level
- 6V to 12V Single Supply Range
- Hysteretic-Logic Thresholds for High-Noise Immunity
- -40℃ to +125℃ Operating Temperature Range
- RoHS Compliant and Halogen Free

APPLICATIONS

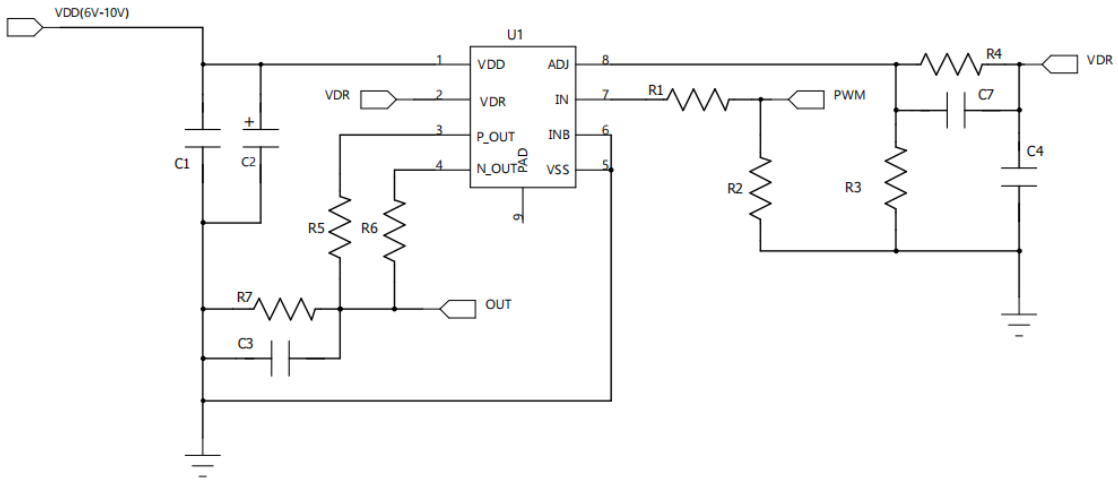
- Boost Converters
- AC/DC,DC/DC Converters
- Flyback and Forward Converters
- Motor Control

DESCRIPTION

The TK1002A is designed to high-speed low-side driver for enhancement mode Gallium Nitride (GaN) transistors and MOSFETs application. With high source and sink output current capability, the TK1002A offers enhanced immunity against Miller turn-on effect.Device Information.

The TX1002A has two separate gate outputs allowing independent adjustment of the turn-on and turn-off capability by adding impedance for gate loop. This part has fast switching speed and minimized propagation delays, facilitating high-frequency operation. The TX1002A can tailor different gate voltage requirements of GaN transistor or MOSFETs through VDRV. The gate driver output voltage level can be adjusted through external resistor voltage divider. The PWM input of this device is CMOS logic compatible and can withstand the input voltage up to 5.5V regardless of the VDRV voltage. This device also supports supply input under voltage lockout.

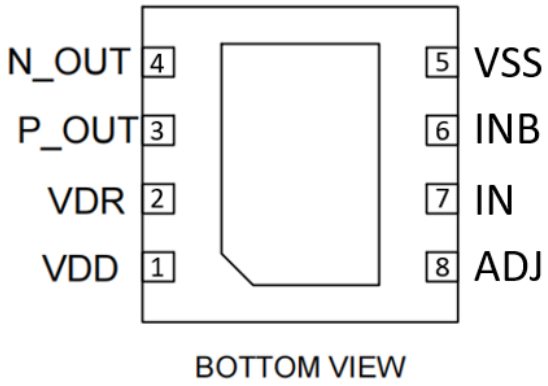
Part Number	Package	Packing
TX1002A	DFN3x3	Tape 3k/reel



Truth Table

IN	INB	P_OUT	N_OUT
L	L	OPEN	L
L	H	OPEN	L
H	L	H	OPEN
H	H	OPEN	L

Pin Configuration and Functions



BOTTOM VIEW

PIN DESCRIPTIONS

Pin No.	Name	Applications Information
1	VDD	Supply Voltage Input. This pin provides bias voltage for the IC. Connect this pin to 6V~12V voltage source and bypass it with an R/C filter.
2	VDRV	Drive Voltage Output. LDO regulated output from VIN to this pin to supply power to gate driver. Connect a MLCC from this pin to GND pin.
3	P_OUT	Connect to the gate of the GaN MOSFET with a short, low inductance path. A gate resistor can be used to adjust the turn-on speed.
4	N_OUT	Connect to the gate of the GaN MOSFET with a short, low inductance path. A gate resistor can be used to adjust the turn-off speed.
5	VSS	All signals are referenced to this ground.
6	INB	Inverting PWM Input. This pin is the PWM input for inverting PWM logic. Connect this pin to the PWM output of the PWM controller.
7	IN	PWM Input. Connect this pin to the PWM output of the PWM controller.
8	ADJ	LDO Output Voltage Adjustment. Connect a resistor voltage divider from VDRV to this pin to set the VDRV output voltage.

Specifications

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	Unit
VDD to GND	-0.3	20	V
VDRV	-0.3	7.5	V
OUTL to GND	-0.3	7.5	V
OUTH to GND	-0.3	7.5	V
PWM,PWMB to GND	-0.3	6V	V
ADJ	-0.3	6V	V
Junction Temperature		+150	°C
Storage Temperature Range	-55	+150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
VDD	6	12	V
VDRV	4.5	5.9	V

Electrical Characteristics

(VDD= 10V, T = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
VDD UVLO Threshold Voltage	$V_{UVLO-VDD}$	Rising	--	3.9	--	V
		Hysteresis	--	0.1	--	V
VDD Quiescent Current	I_{Q-VDD}	PWM = PWMB = 0V, VDRV = open	--	300	--	uA
VDRV Voltage						
VDRV UVLO Threshold Voltage	$V_{UVLO-VDRV}$	Rising	3.9	4.0	4.1	V
		Hysteresis	--	0.3	--	
VDRV Output Current	I_{VDRV}		50	--	--	mA
VDRV Dropout Voltage	$V_{DROP-DRV}$	VIN=5.5V, VDRV set to 6V, I_{VDRV} = 20mA	--	100	--	mV
ADJ						
ADJ Voltage	V_{ADJ}		1.2	1.25	1.3	V
High-side Sourcing Output (OUTH)						
Driver Output Resistance - Pulling Up	$R_{DS(ON)-P}$	VDRV = 6V, I_{OUTH} = 100mA	--	2.5	--	Ω
Source Peak Current	I_{SRC}	C_L = 0.22uF, F_{SW} = 1 kHz	--	-1.7	--	A
Output Rise Time	t_R	VDRV = 6V, C_L = 1nF	--	13.4	--	ns
Turn-On Propagation Delay	t_{D-ON}	VDRV = 6V, C_L=1nF	--	11	35	ns
Low-side Sourcing Output (OUTL)						
Driver Output Resistance - Pulling Down	$R_{DS(ON)-N}$	VDRV = 6V, I_{OUTL} = -100mA	--	0.55	--	Ω
Sink Peak Current	I_{SNK}	C_L = 0.22uF, F_{SW} = 1 kHz	--	2	--	A
Output Fall Time	t_F	VDRV = 6V, C_L = 1nF	--	8.4	--	ns
Turn-Off Propagation Delay	t_{D-OFF}	VDRV = 6V, C_L=1nF	--	11	35	ns
PWM Input						
Input High Level	PWM_H	V_{LDO5} = 5V	2.2	--	--	V
Input Low Level	PWM_L	V_{LDO5} = 5V	--	--	0.5	V
Input Pull Down Resistance	RI		--	400	--	kΩ
Output Pulse						
Minimum Off Time	T_{min_off}	V_{DRV}=6V, C_L=1nF	--	40	--	ns

Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_R	Rise time	C_L = 1000 pF		13.4		ns
t_F	Fall time	C_L = 1000 pF		8.4		ns
t_{D-ON}	Turnon propagation delay	C_L = 1000 pF		11		ns
t_{D-OFF}	Turnoff propagation delay	C_L = 1000 pF		11		ns

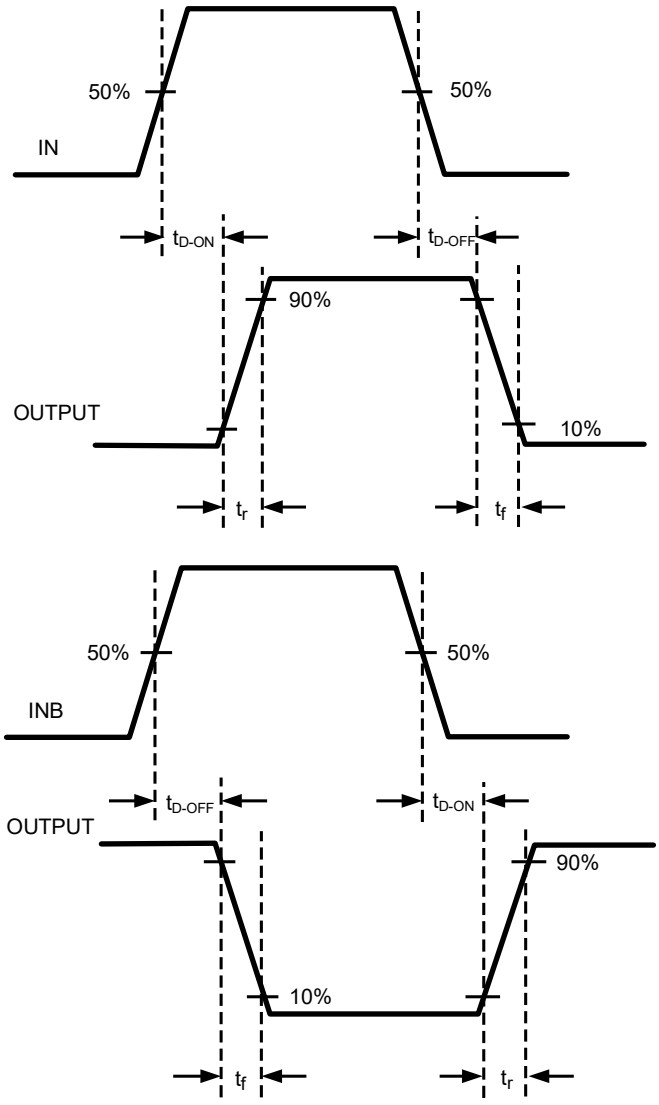
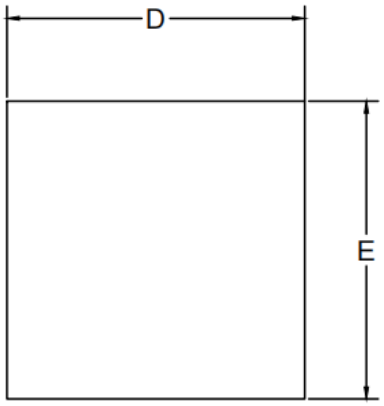


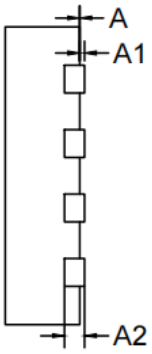
Figure 1. Timing Diagram

Package Outline Dimensions

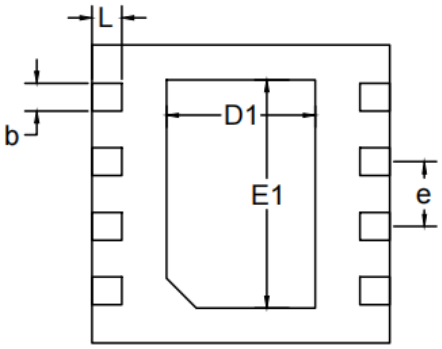
尺寸对照表Dimensions(mm)			
符号Symbol	最小值Min	典型值Typ	最大值Max
A	0.70	0.75	0.8
A1	-	-	0.05
A2	REF 0.203		
b	0.23	0.28	0.33
D	2.9	3	3.1
D1	1.4	1.5	1.6
E	2.9	3	3.10
E1	2.2	2.3	2.40
e	TYP 0.65		
L	0.25	0.3	0.35



TOP VIEW



SIDE VIEW



BOTTOM VIEW

DFN3x3-8