Description

The TESD05LCT2B is an ultra-low capacitance ESD array that employs advanced monolithic silicon technology to deliver fast response times and low ESD clamping voltages. This makes it an ideal solution for protecting voltage-sensitive high-speed data lines. With an ultra-low typical capacitance of 0.6 pF and compliance with the IEC 61000-4-2 (ESD) standard (±20kV air and ± 15kV contact discharge), it is packaged in a 6-pin lead-free SOT-23-6 package. Its compact size, ultra-low capacitance, and high ESD surge capability make it suitable for multimedia and other high-speed port applications.

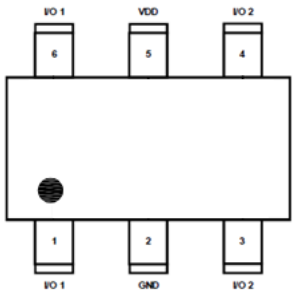
Features

Ultra-low capacitance: 0.6pF typical (I/O-GND)
Ultra-low leakage: nA level
Low operating voltage: 5.0V
Protects up to 4 data lines and one power line
Low clamping voltage
Complies with:
--IEC 61000-4-2 (ESD) immunity test (Air: ±20kV; Contact: ±15kV)
--IEC 61000-4-5 (Lightning): 4.5A (8/20μs)
SOT-23-6 Package
RoHS Compliant

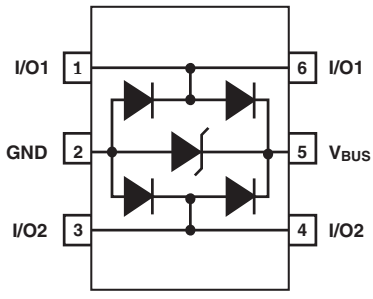
Applications

Monitors and flat panel displays
Set-top boxes and Digital TVs
Video graphics cards
Digital Video Interface (DVI)
Notebook computers
PCI Express and Serial SATA Ports

Marking Diagram



Circuit Diagram



Ordering Information

DEVICE	PACKAGE
TESD05LCT2B	3000/Tape & Reel

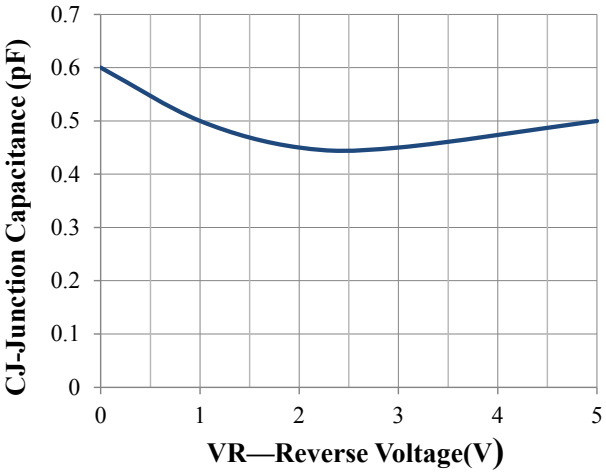
Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter	Symbol	Value	Unit
Peak Pulse Power (8/20μs,I/O-GND)	Ppk	60	W
Peak Pulse Power (8/20μs,Vcc-GND)	Ppk	300	W
Peak Pulse Current (8/20μs,I/O-GND)	IPP	4.5	A
Peak Pulse Current (8/20μs,Vcc-GND)	IPP	17	A
ESD per IEC 61000−4−2 (Air) ESD per IEC 61000−4−2 (Contact)	$V_{ESD,VDD}$ $V_{ESD,I/O}$	±20 ±15	kV
Operating Temperature Range	TJ	−55 to +125	°C
Storage Temperature Range	Tstg	−55 to +150	°C

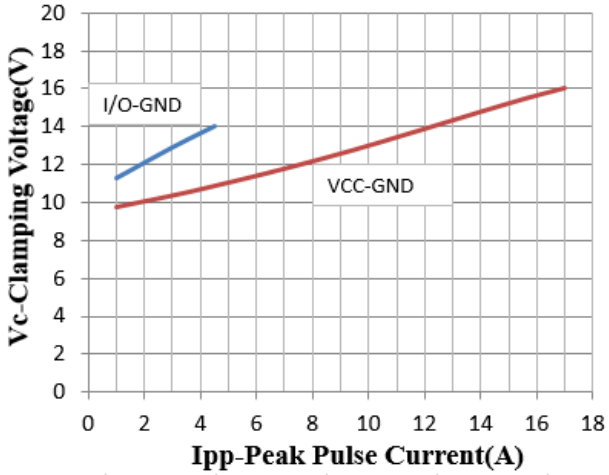
Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	Pin 5 to GND,I/O-GND			5. 0	V
Breakdown Voltage	V_{BR}	I_T = 1mA($_{Pin\ 5\ to\ GND,I/O-GND}$)	6.0	7.5	8.5	V
Reverse Leakage Current	I_R	V_{RWM} = 5. 0V			0.5	μA
Forward Breakdown Voltage	V_F	I_F = 15mA,GND to Pin 5/IO		0.8	1.0	V
Clamping Voltage	V_C	IPP = 4.5A (8 x 20μs pulse, I/O to GND)		14.0	15.0	V
Clamping Voltage	V_C	IPP = 17A (8 x 20μs pulse,Pin 5 to GND)		16.0	18. 0	V
Junction Capacitance	C_J	V_{pin5} = 5V, I/O=0V, f = 1MHz,I/O-GND		0.6	0.7	pF
Junction Capacitance	C_J	V_{pin5} = 5V, I/O=0V, f = 1MHz,I/O-I/O pins		0.3	0.4	pF

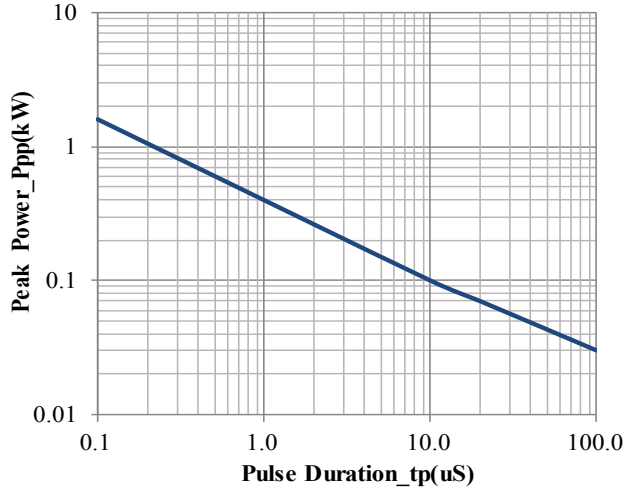
Typical Characteristics



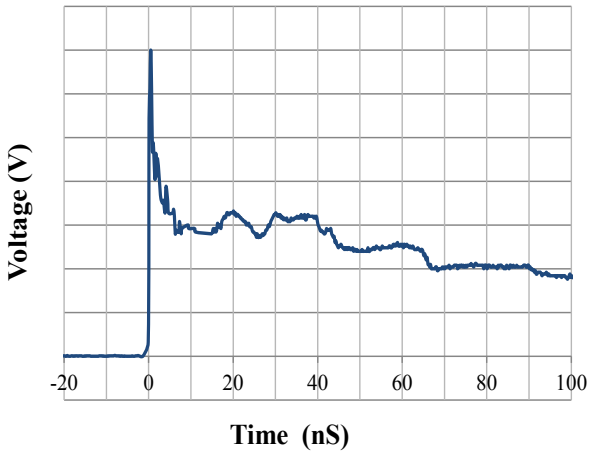
Junction Capacitance vs. Reverse Voltage



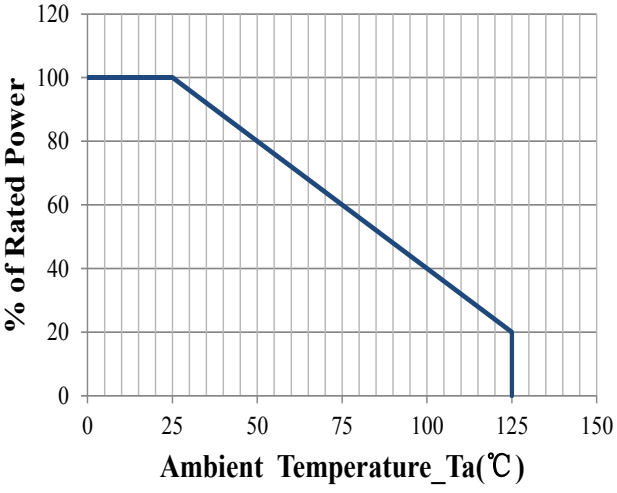
Clamping Voltage vs. Peak Pulse Current



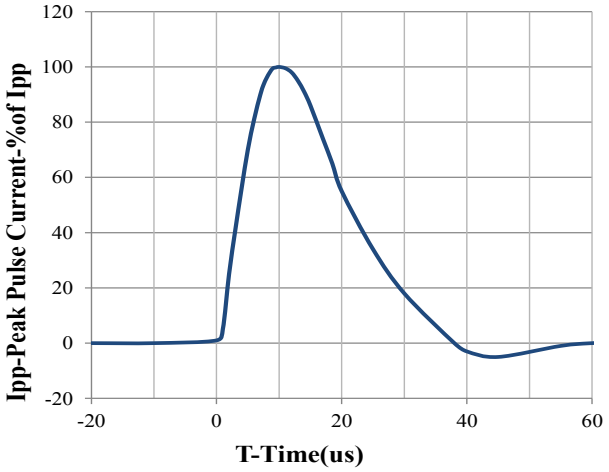
Peak Pulse Power vs. Pulse Time



IEC61000−4−2 Pulse Waveform

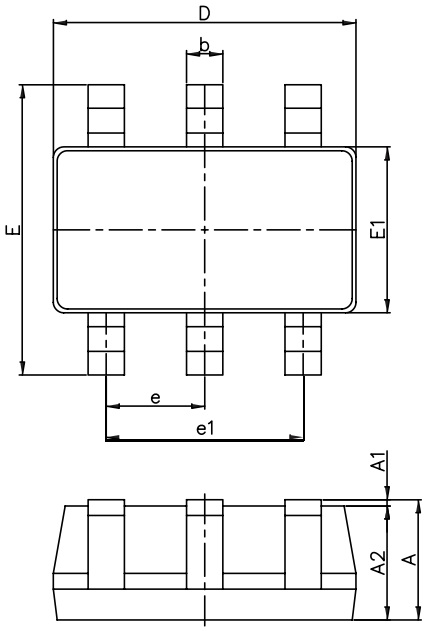


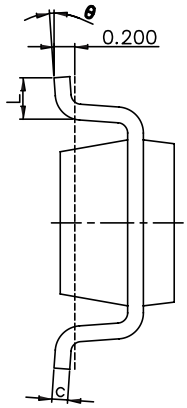
Power Derating Curve



8 X 20us Pulse Waveform

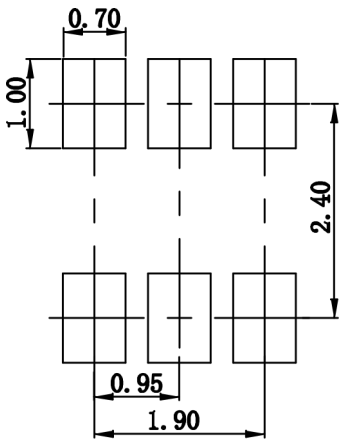
SOT-23-6L Package Outline Dimensions





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

SOT-23-6L Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.